Photobit

PB-MV13
20mm CMOS Active-Pixel Digital Image Sensor

Written and designed at Photobit Corporation, 135 North Los Robles Avenue, 7th Floor, Pasadena, California 91101, U.S.A.
Telephone (626) 683-2200. Fax (626) 683-2220. www.photobit.com

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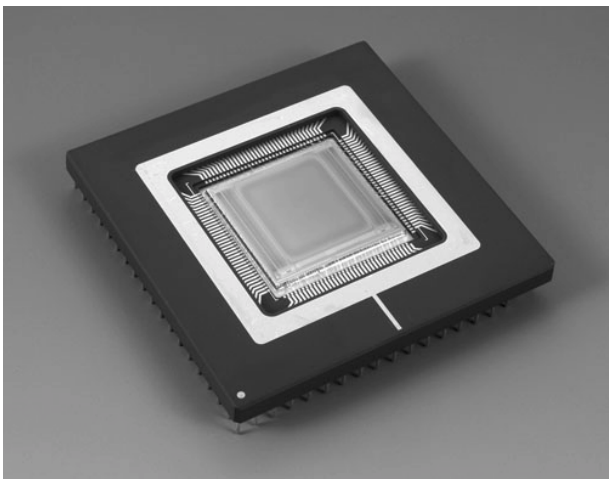


1.0 Introduction

- Photons-to-bits data stream
- 1280H x 1024V image resolution
- TrueSNAP™ (Shuttered-Node Active Pixel) freeze-frame electronic shutter
- 500+ frames per second
- 12-micron square active pixels
- Monochrome or color
- 10 parallel digital output ports
- <500 mW maximum power dissipation @ 500 fps
- On-chip TrueBit® Noise Cancellation
- Photobit® TrueColor™ Image Fidelity
- On-chip 10-bit analog-to-digital converters
- 3.3-volt operation

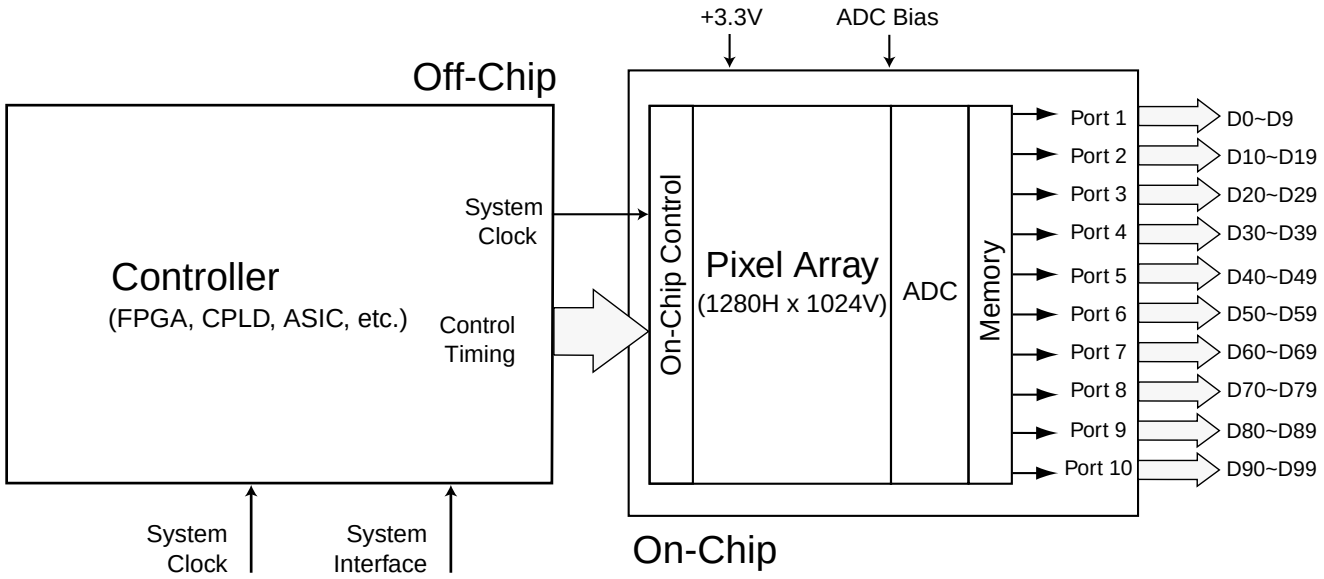
1.1 Features

The PB-MV13 is a 1280H x 1024V (1.31 megapixel) CMOS digital image sensor capable of 500 frames-per-second (fps) operation. Its TrueSNAP™ electronic shutter allows simultaneous exposure of the entire pixel array. Available in color or monochrome, the sensor has on-chip 10-bit analog-to-digital converters (ADCs), which are self-calibrating, and a fully digital interface. The chip's input clock rate is 66 MHz at approximately 500 fps, providing compatibility with many off-the-shelf interface components.

The sensor has ten (10) 10-bit-wide digital output ports. Its open architecture design provides access to internal operations. ADC timing and pixel-read control are integrated on-chip. At 60 fps, the sensor dissipates less than 150 mW, and at 500 fps less than 500 mW; it operates on a 3.3V supply. Pixel size is 12 microns square and digital responsivity is 1000 bits per lux-second.

The PB-MV13 CMOS image sensor has an open architecture to provide access to its internal operations. A complete camera system can be built by using the chip in conjunction with the following external devices:

- An FPGA/CPLD/ASIC controller, to manage the timing signals needed for sensor operation.
- A 20mm diagonal lens.
- Biasing circuits and bypass capacitors.

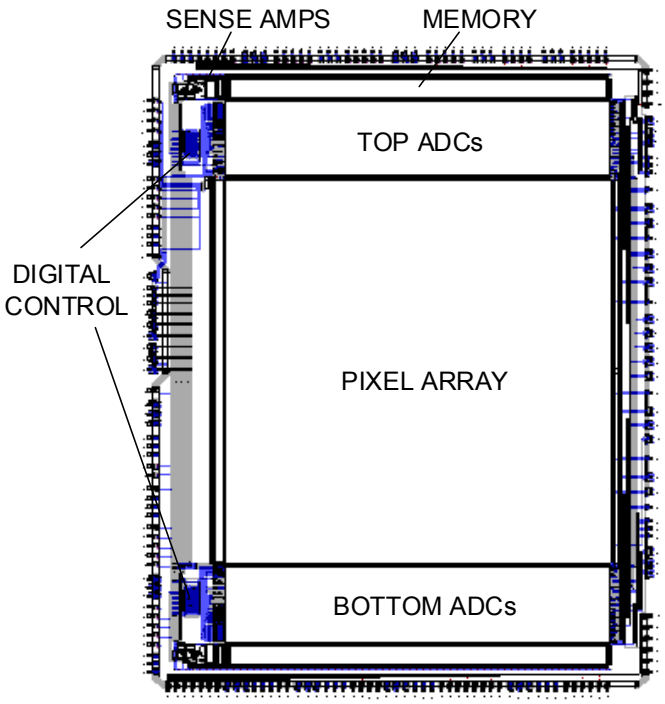


A Camera System Using the PB-MV13 CMOS Image Sensor

1.2 Top-Level Specification

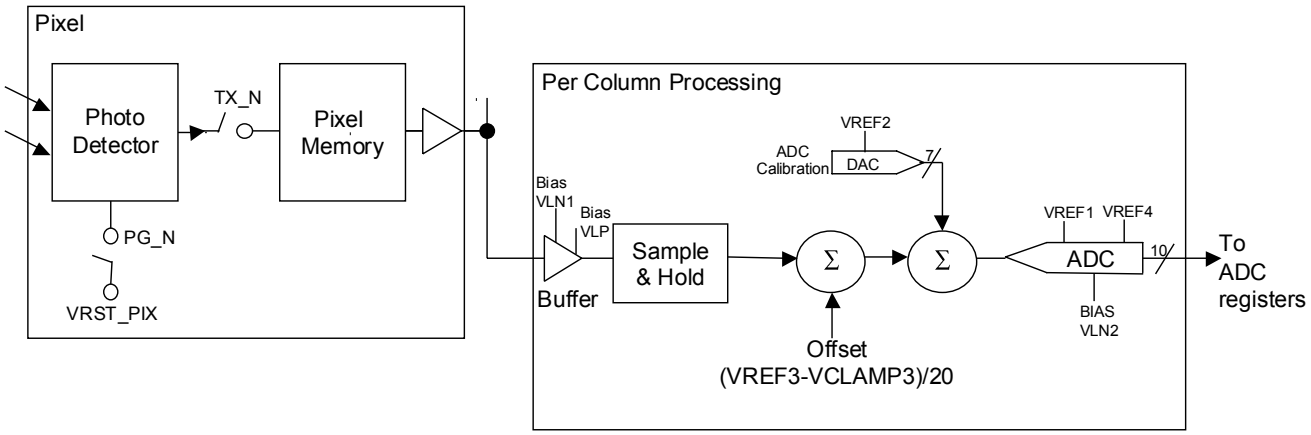
Array Format	1280H x 1024V (1,310,720 pixels) 5:4 aspect ratio
Pixel Size and Type	12.0 µm x 12.0 µm TrueSNAP™ (Shuttered-Node Active Pixel)
Sensor Imaging Area	H: 15.36 mm, V: 12.29 mm, Diagonal: 19.67 mm
Frame Rate	0-500+ fps @ (1280 x 1024) >10,000 fps with partial scan [e.g. 0-4000 fps @ (1280 x 128)]
Output Data Rate	660 Mbytes/sec. (master clock 66 MHz, ~500 fps)
Power Consumption	<500 mW @ 500 fps <150 mW @ 60 fps
Digital Responsivity	Monochrome: 1000 bits per lux-second @ 550 nm ADC reference @ 1V
Internal Intra-Scene Dynamic Range	59 dB
Supply Voltage	+3.3 V
Operating Temperature	-5°C to +60°C
Output	10-bit digital through 10 parallel ports
Color	Monochrome or color RGB
Shutter	Photobit® TrueSNAP™ freeze-frame electronic shutter
Shutter Efficiency	>99.9%
Shutter Exposure Time	10 µsec to greater than 33 msec
ADC	On-chip 10-bit column-parallel
Package	280-pin ceramic PGA or 208-pin CQFP
Programmable Controls	Open architecture On-chip: • ADC controls • Output multiplexing • ADC calibration Off-chip: • Window size and location • Frame rate and data rate • Shutter exposure time (integration time) • ADC reference

2.0 Electrical

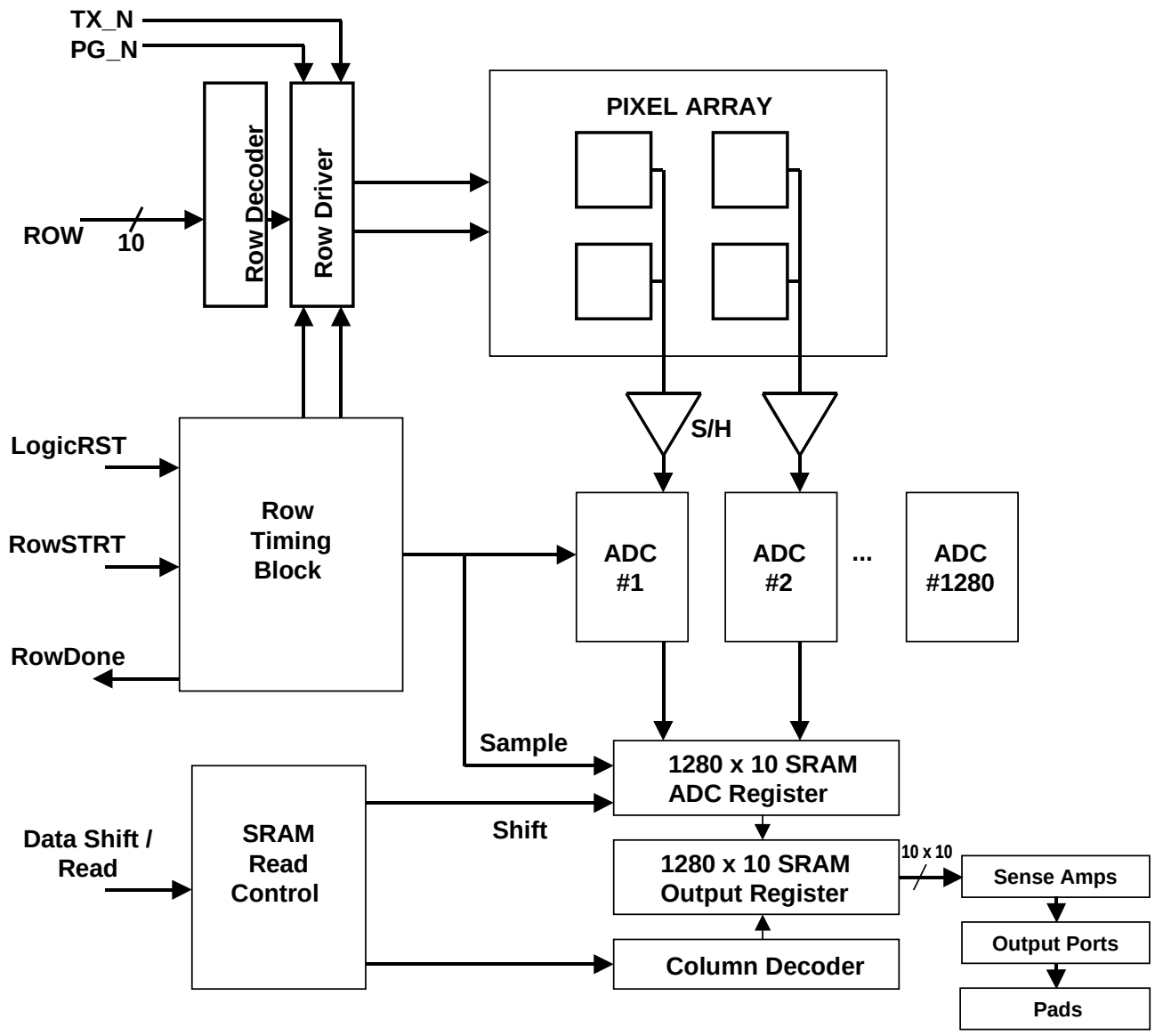


Sensor Architecture (not to scale)

2.1 Signal Path Diagram



2.2 Functional Block Layout



2.3 External Control Sequence

The PB-MV13 includes on-chip timing and control circuitry to control most of the pixel, ADC, and output multiplexing operations. However, the sensor still requires a controller (FPGA, CPLD, ASIC, etc.) to guide it through the full sequence of its operation.

With the TrueSNAP™ freeze-frame electronic shutter signal charges are integrated in all pixels in parallel. The charges are then sampled into pixel analog memories (one memory per pixel) and subsequently, row by row, are digitized and read out of the sensor. The integration of photosignal is controlled by two control signals: PG_N and TX_N. To clear pixels and start new integration, PG_N is made low. To transfer the data into pixel memory, TX_N is made low. The time difference between the two procedures is the exposure time. It should be noted that neither the PG_N or TX_N pulses clear the pixel analog memory. Pixel memory can be cleared during the previous readout (i.e., the readout process resets the pixel analog memory), or by applying PG_N and TX_N together (i.e., clearing both pixel and pixel memory at the same time).

With the TrueSNAP™ freeze-frame electronic shutter the sensor can operate in either simultaneous or sequential mode in which it generates continuous video output. In simultaneous mode, as a series of frames are being captured, the PG_N and TX_N signals are exercised while the previous frame is being read out of the sensor. In simultaneous mode typically the “end of integration” occurs in the last row of the frame (row #1023) or in the last row of the window of interest. The position of the “start integration” is then calculated from the desired integration time. In sequential mode the PG_N and TX_N signals are exercised to control the integration time, and then digitization and readout of the frame takes place. Alternatively, the sensor can run in single frame or snap-shot mode in which one image is captured.

The sensor has a column-parallel ADC architecture that allows the array of 1,280 analog-to-digital converters on the chip to digitize simultaneously the analog data from an entire pixel row. The following input signals are utilized to control the conversion and readout process:

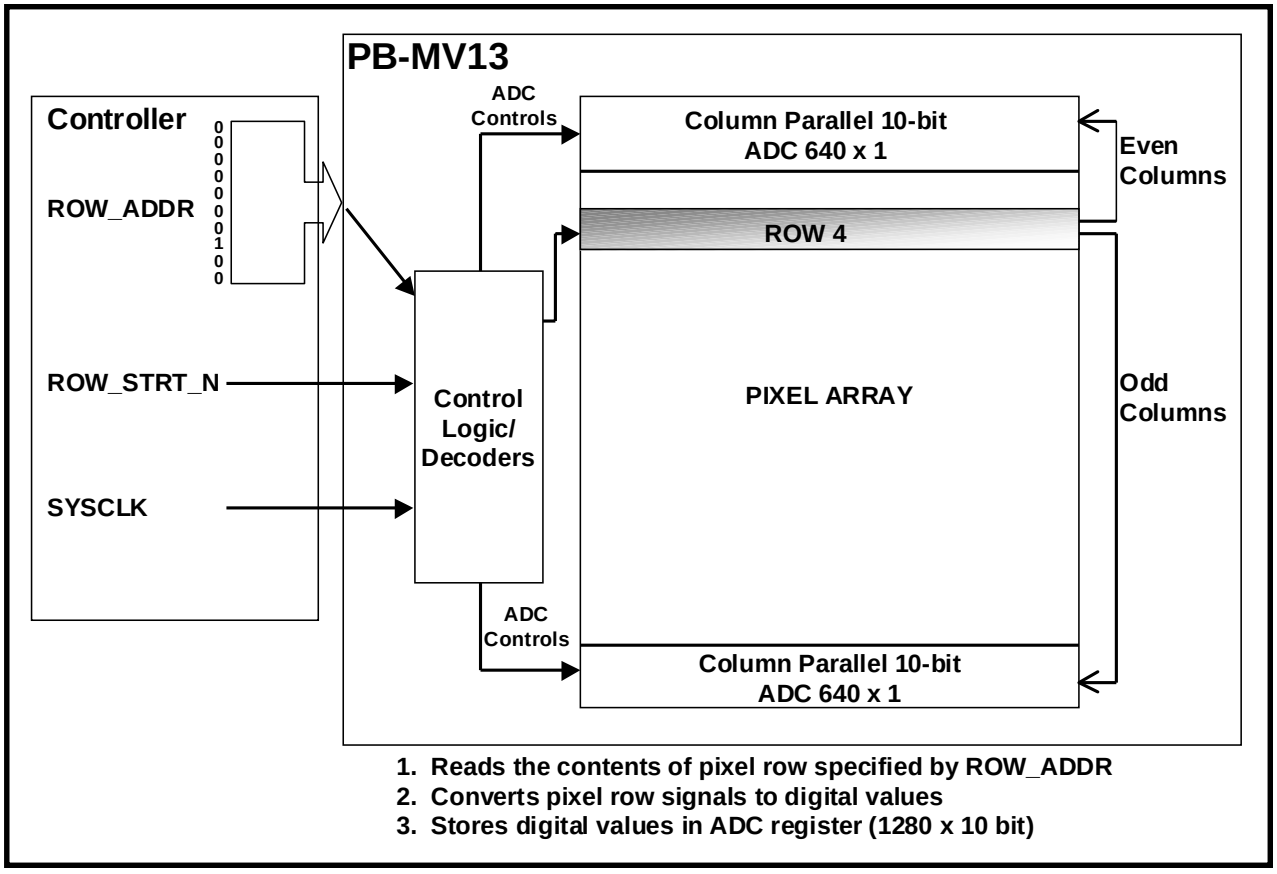
Signal Name	Description	Input Bus Width
ROW_ADDR	Row Address	10-bit
ROW_STRT_N	Row Start	1-bit
LD_SHFT_N	Load shift register	1-bit
DATA_READ_EN_N	Data read enable	1-bit

The 10-bit ROW_ADDR (row address) input bus selects the pixel row to be read for each readout cycle. The ROW_STRT_N signal starts the process of reading the analog data from the pixel row, the analog-to-digital conversion, and the storage of the digital values in the ADC registers. When these actions are completed, the sensor sends a response back to the system controller using the ROW_DONE_N. Row address must be valid for the first half of the row processing time (the period between ROW_START_N and ROW_DONE_N).

The PB-MV13 contains a pipeline style memory array, which is used to store the data after digitization. This memory also allows the data from the previous row conversion cycle to be read while a new conversion is taking place.

The digital readout is controlled by lowering the LD_SHFT_N signal, followed by the DATA_READ_EN_N signal. LD_SHFT_N transfers the digitized data from the ADC register to the output register. DATA_READ_EN_N is used to enable the data output from the output register. A new pixel row readout and conversion cycle can be started two clock cycles after DATA_READ_EN_N is pulled low. The output register allows the reading of the digital data from the previous row to be performed at the same time as a new conversion (pipeline mode). This means that the total row time will be only that between when: (a) the ROW_STRT_N signal is applied and ROW_DONE_N is returned; and (b) LD_SHFT_N and DATA_READ_EN_N are applied plus two clock cycles. The pipelined operation means there will always be 1 row of latency at the start of sensor operation. The alternative to pipelined operation is burst data operation in which a new pixel row conversion is not initiated until after the output register is emptied (and LD_SHFT_N has been taken high). The ratio of line active and blanking times can be adjusted to easily match a variety of display and collection formats.

2.3 External Control Sequence (continued)



Example 1 - Row 4 of the PB-MV13 being digitized

ⓐ PG_N and TX_N

To start integration, the PG_N signal simultaneously resets the photodetectors for the entire pixel array. To end integration, the TX_N signal simultaneously transfers charge from photodetector to memory inside each pixel for the entire pixel array. *In sequential mode the PG_N and the TX_N pulses must have a minimum duration of 64 SYSCLK cycles. In simultaneous mode the PG_N and TX_N pulses must have a duration of 64 SYSCLK cycles and be applied in the window between the 66th and 129th SYSCLK cycles. Additionally, in simultaneous mode between exposures a single SYSCLK duration pulse must be applied each row during the 130th clock cycle.*

ⓑ ROW_ADDR

The address for the pixel row to be read is input externally via this 10-bit input bus. *Must be valid for at least 66 SYSCLK cycles, must be valid when ROW_STRT_N is pulled low.*

ⓒ ROW_STRT_N

This signal:

i-Reads the contents of the pixel row specified by ROW_ADDR (ⓑ above)

ii-Converts pixel row signal to digital value

iii-Stores digital value in ADC register (1280 x 10-bit)

This process is completed in 128-129 SYSCLK cycles. Must be valid for a minimum of two clock cycles and a maximum of 100 clock cycles.*

ⓓ ROW_DONE_N

128-129* SYSCLK cycles after ROW_STRT_N has been pulled low (ⓒ above) the sensor acknowledges the completion of a row read operation/digitization by sending out a low going pulse on this pin. V*alid for two clock cycles.*

ⓔ LD_SHFT_N

This signal transfers the digitized data from the ADC register to the output register (1280 x 10-bit) and gates the power to the sense amplifiers. The first data (columns 1-10) are available for output at the third rising edge of SYSCLK after LD_SHFT_N is pulled low. *May be enabled simultaneously with or after the rising edge of ROW_DONE_N. Must remain low the entire time the data is being read out.*

ⓕ DATA_READ_EN_N

This signal is used to enable the data output from the output register (1280 x 10-bit) to the ten, 10-bit output ports. *May be initiated simultaneously with or after LD_SHFT_N is selected. Minimum width is one clock cycle.*

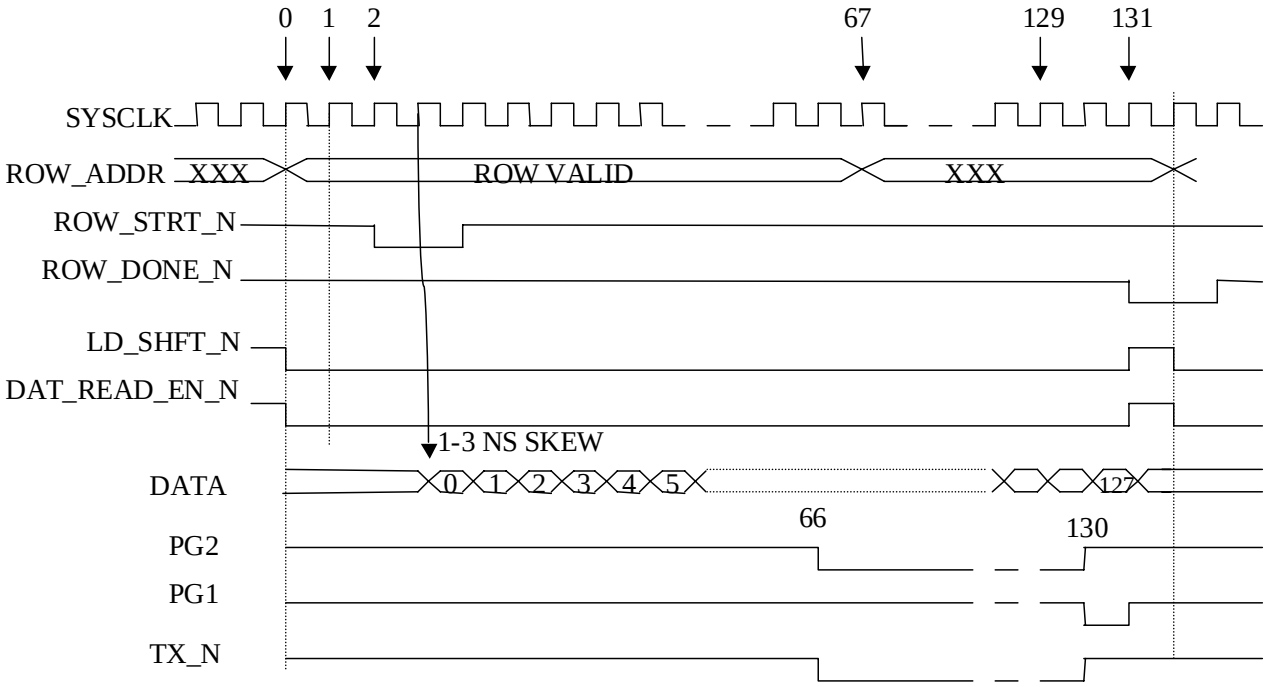
ⓖ The pixel array of the PB-MV13 image sensor is vertically partitioned into 128 groups of 10 columns that correspond to the sensor's ten (10) identical output ports.The first column of each 10-column set always goes to Port 1, while the last column of each set goes to Port 10, etc. The operator can access all pixels of the PB-MV13 only by using all of its ports (see page 4).

	CLK 1	CLK 2 ..... CLK128
Port 1	Col. 1	Col. 11 .... Col. 1271
Port 2	Col. 2	Col. 12 .... Col. 1272
Port 3	Col. 3	Col. 13 .... Col. 1273
Port 4	Col. 4	Col. 14 .... Col. 1274
Port 5	Col. 5	Col. 15 .... Col. 1275
Port 6	Col. 6	Col. 16 .... Col. 1276
Port 7	Col. 7	Col. 17 .... Col. 1277
Port 8	Col. 8	Col. 18 .... Col. 1278
Port 9	Col. 9	Col. 19 .... Col. 1279
Port 10	Col. 10	Col. 20 .... Col. 1280

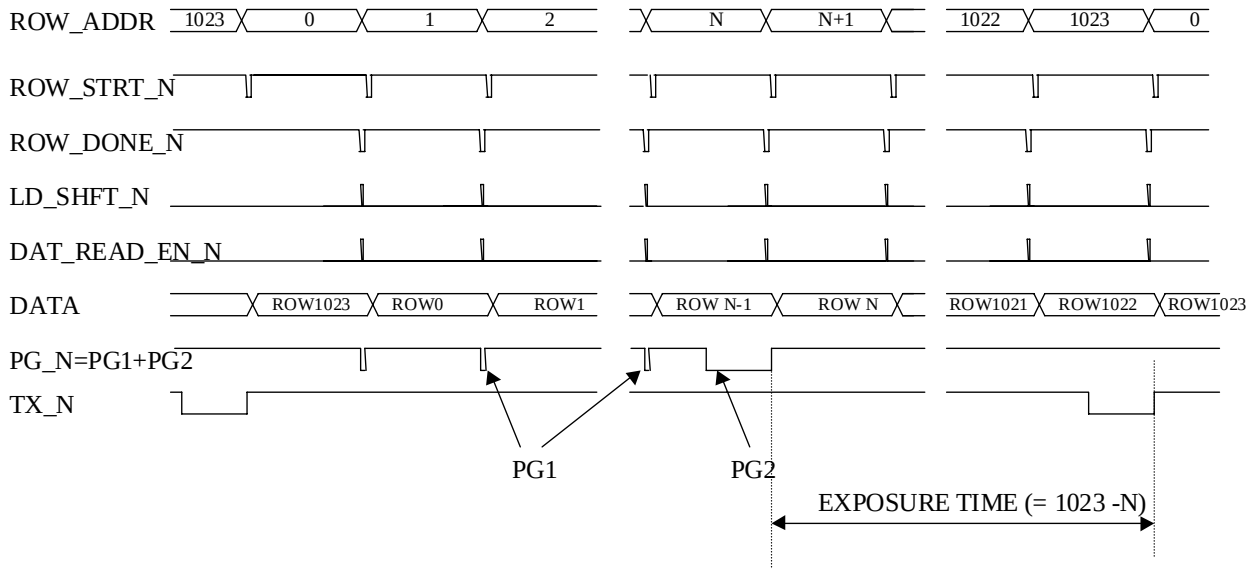
ⓗ The use of an output register allows the processing of a row to be performed while the digital data from the previous operation is being read out of the sensor. A new pixel readout and conversion cycle can be started two clock cycles after DATA_READ_EN_N is pulled low.

*In order to minimize the sensor power consumption, the row processing circuitry operates at SYSCLK÷2. Therefore, depending on the user's implementation, there will be either 128 or 129 SYSCLK cycles between the start of ROW_STRT_N and ROW_DONE_N.

2.3 External Control Sequence (continued)

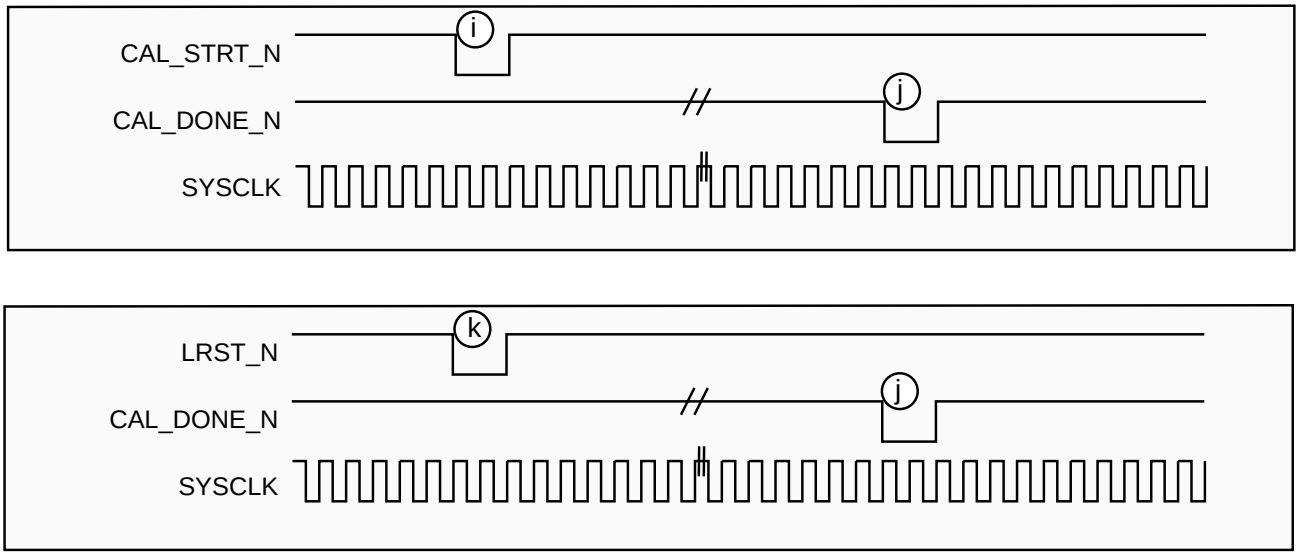


Timing diagram for one row



Frame Timing

The PB-MV13 contains special self-calibrating circuitry that enables it to reduce its own column-wise fixed-pattern noise. This calibration process consists of connecting a calibration signal (VREF2) to each of the ADC inputs, and estimating and storing these offsets (7 bits) to subtract from subsequent samples. The Typical I/O Signal Timing (Initialization Sequence) diagram shows the timing sequence to calibrate the sensor. Calibration occurs automatically after logic reset (LRST_N) but it can also be started by the user, by pulling CAL_STRT_N low. When calibration is finished, the sensor generates the active low CAL_DONE_N. Significant ambient temperature drift may justify recalibration.



Typical I/O Signal Timing (Initialization Sequence)

ⓘ CAL_STRT_N is a two-clock cycle-wide active-low pulse that initiates the ADC calibration sequence. The pulse must not be actuated for 1 microsecond after either power-up or removal of the sensor from a power-down state. Users may find it easiest to calibrate by means of the logic reset.

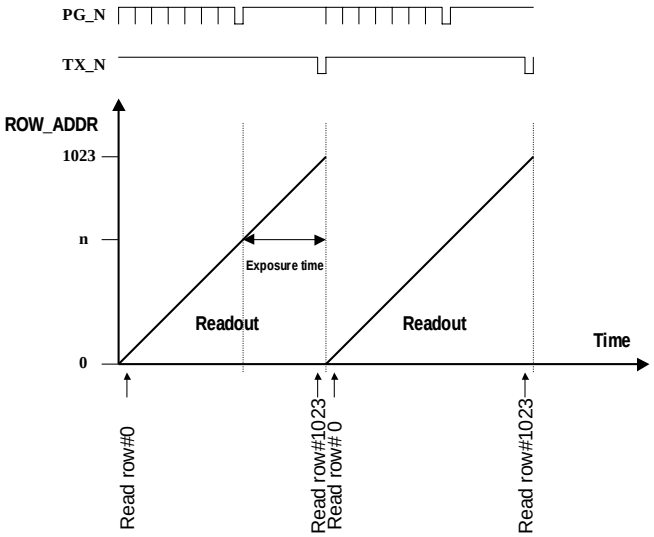
ⓙ CAL_DONE_N is a two-clock cycle-wide active-low output pulse that is asserted when the ADC calibration is complete. The device will automatically initiate a calibration sequence upon a logic reset. Completion of this sequence, in cases where it is initiated by a reset, is still with the CAL_DONE_N signal. This process is complete within 112 SYSCLK cycles of CAL_STRT_N. This process is complete within 112 SYSCLK cycles of LRST_N.

ⓚ LRST_N is a two-clock cycle-wide active-low pulse that resets the digital logic. It puts all logic into a known state (all flip-flops are reset). This signal also initiates an ADC calibration sequence.

2.4 Electronic Shutter

The PB-MV13 is intended to be operated primarily with the TrueSNAP™ freeze-frame electronic shutter, but is also capable of operating in Electronic Rolling Shutter (ERS) mode. With TrueSNAP the shutter can be operated to generate continuous video output (simultaneous mode or sequential mode) or caputre single images (single frame mode).

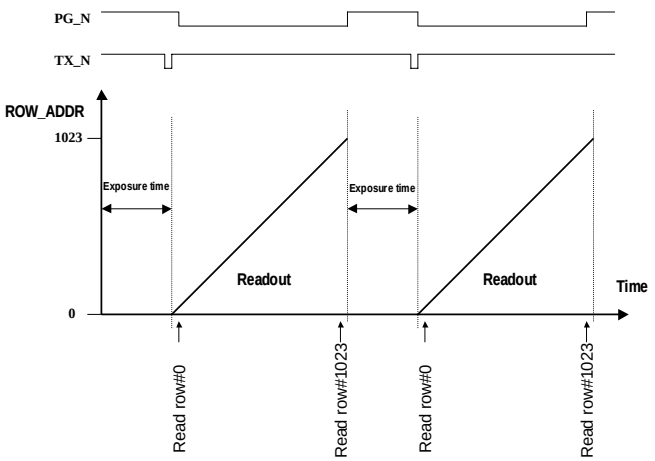
2.4.1 TrueSNAP™ Simultaneous Mode



Typical Example of TrueSNAP Sequential Mode: Exposure Followed by Readout

In simultaneous mode, as a series of frames are being captured, the PG_N and TX_N signals are exercised while the previous frame is being read out of the sensor. In simultaneous mode typically the "end of integration" occurs in the last row of the frame (row #1023) or in the last row of the window of interest. The position of the "start integration" is then calculated from the desired integration time. Please note that pixel memory is cleared during readout process.

2.4.2 TrueSNAP™ Sequential Mode

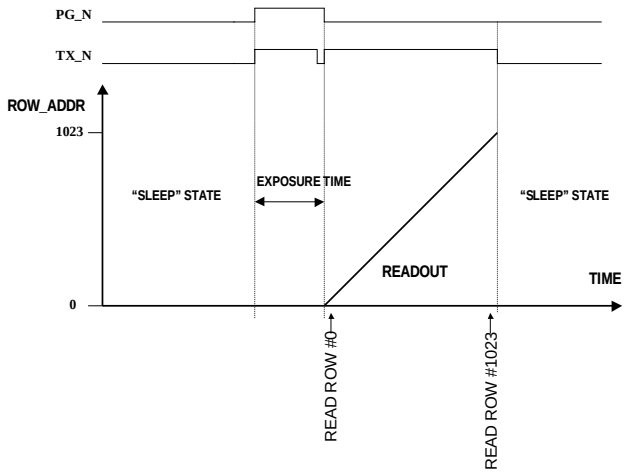


Typical Example of TrueSNAP Simultaneous Mode: Exposure During Readout

In sequential mode the PG_N and TX_N signals are exercised to control the integration time, and then digitization and readout of the frame takes place. Please note that pixel memory is cleared during readout process.

2.4.3 TrueSNAP™ Single Frame

The PB-MV13 can run in single frame or snap-shot mode in which one image is captured. In single frame mode integration must be preceded wth a void frame read (selecting all addresses and applying ROW_STRT_N) or PG_N and TX_N must be applied together to clear pixel and pixel memory.



Typical Example of TrueSNAP Single-Frame Mode

2.4.4 ERS Mode

This mode is enabled by pulling PG_N high and TX_N low. A detailed description of ERS mode can be found in Section 2.4 of the PB-1024 Product Specification.

2.4.5 Partial Scan Examples

The PB-MV13 can be partially scanned by sub-sampling rows. The user may select which rows and how many rows to include in a partial scan. For example, with a 66-megahertz clock, a row time is approximately 2 microseconds, resulting in the following possiblities:

1 row in frame: 500,000 frames per second
2 rows in frame: 250,000 frames per second
10 rows in frame: 50,000 frames per second
100 rows in frame: 5,000 frames per second
256 rows in frame: 2,000 frames per second
512 rows in frame: 1,000 frames per second
1,024 rows in frame: 500 frames per second
...etc

2.5 Pin Descriptions

Signal Name	Function	Pin Number(s)
VAA	Power supply for analog processing circuitry (column buffers, ADC, and support).	R18, P18, K18, J18
AGND	Ground for analog signal processing circuitry.	T17, N16, L17, K17, J15, R17
CAL_DONE_N	A two-clock cycle-wide active-low pulse that indicates the ADC has completed its calibration operation.	L3
CAL_STRT_N	Starts the calibration process for the ADC. This is a two-clock cycle-wide active-low pulse.	L2
DARK_OFF_EN_N	A low input enables common mode dark offset to all pixels. The value of the offset is defined by VREF3 and VCLAMP3. Subtracts a fixed offset pre-ADC. Signal is pulled up on-chip.	F1
DATA [99:0]	Pixel data output bus that is ten pixels (100 bits) wide. Bit 0 is the LSB (least significant bit) of the lowest order pixel (see page 10 ⓖ and drawing on page 4). In the group of ten pixels being output, bit 9 is the MSB (most significant bit).	
DATA0		T13
DATA1		U14
DATA2		V15
DATA3		T14
DATA4		V16
DATA5		T15
DATA6		U16
DATA7		R14
DATA8		V18
DATA9		P15
DATA10		D14
DATA11		A16
DATA12		C16
DATA13		E13
DATA14		D15
DATA15		A18
DATA16		E14
DATA17		B18
DATA18		D17
DATA19		E16
DATA20		W11
DATA21		U10
DATA22		V11
DATA23		R11
DATA24		V12
DATA25		W13
DATA26		U12
DATA27		V13
DATA28		R12

Signal Name	Function	Pin Number(s)
DATA29		V14
DATA30		B11
DATA31		C12
DATA32		A12
DATA33		B12
DATA34		E11
DATA35		B13
DATA36		C14
DATA37		D13
DATA38		E12
DATA39		C15
DATA40		U6
DATA41		V7
DATA42		T8
DATA43		R9
DATA44		V8
DATA45		U8
DATA46		V9
DATA47		T9
DATA48		V10
DATA49		R10
DATA50		C8
DATA51		A7
DATA52		D9
DATA53		E9
DATA54		A8
DATA55		C10
DATA56		A9
DATA57		D10
DATA58		B10
DATA59		C11
DATA60		T4
DATA61		R6
DATA62		V3
DATA63		W3
DATA64		R7
DATA65		W4
DATA66		T6
DATA67		V5
DATA68		R8
DATA69		V6
DATA70		E6
DATA71		D5
DATA72		C5

2.5 Pin Descriptions (continued)

Signal Name	Function	Pin Number(s)
DATA73		D6
DATA74		A3
DATA75		C6
DATA76		D7
DATA77		A5
DATA78		E8
DATA79		A6
DATA80		M5
DATA81		P2
DATA82		N3
DATA83		T1
DATA84		P3
DATA85		U1
DATA86		P4
DATA87		T2
DATA88		V1
DATA89		R4
DATA90		H5
DATA91		E3
DATA92		E2
DATA93		D1
DATA94		D3
DATA95		E4
DATA96		C2
DATA97		A1
DATA98		F5
DATA99		B2
VDD	Power supply for core digital circuitry.	J4, N15, J16
DGND	Ground for core digital circuitry.	H3, H18, T18
LD_SHFT_N	An active-low envelope signal that places the recently converted row of data into output register for output, enables the sense amps and resets the column counter.	K2
DATA_READ_EN_N	An active-low envelope signal that enables the column counter and causes the ten (10) 10-bit output ports to be updated with data on the rising edge of the system clock. Column counter is disabled and output is frozen when this input is high.	J3
LRST_N	Global logic reset function (asynchronous). Active-low pulse.	L1
ROW_ADDR [9:0]	10-bit bus (0 to 1023, bottom to top) that controls which pixel row is being processed or read out. An asychronous (unclocked) digital input. Bit 9 is the MSB.	
ROW_ADDR0		G18
ROW_ADDR1		H16
ROW_ADDR2		H15
ROW_ADDR3		F18

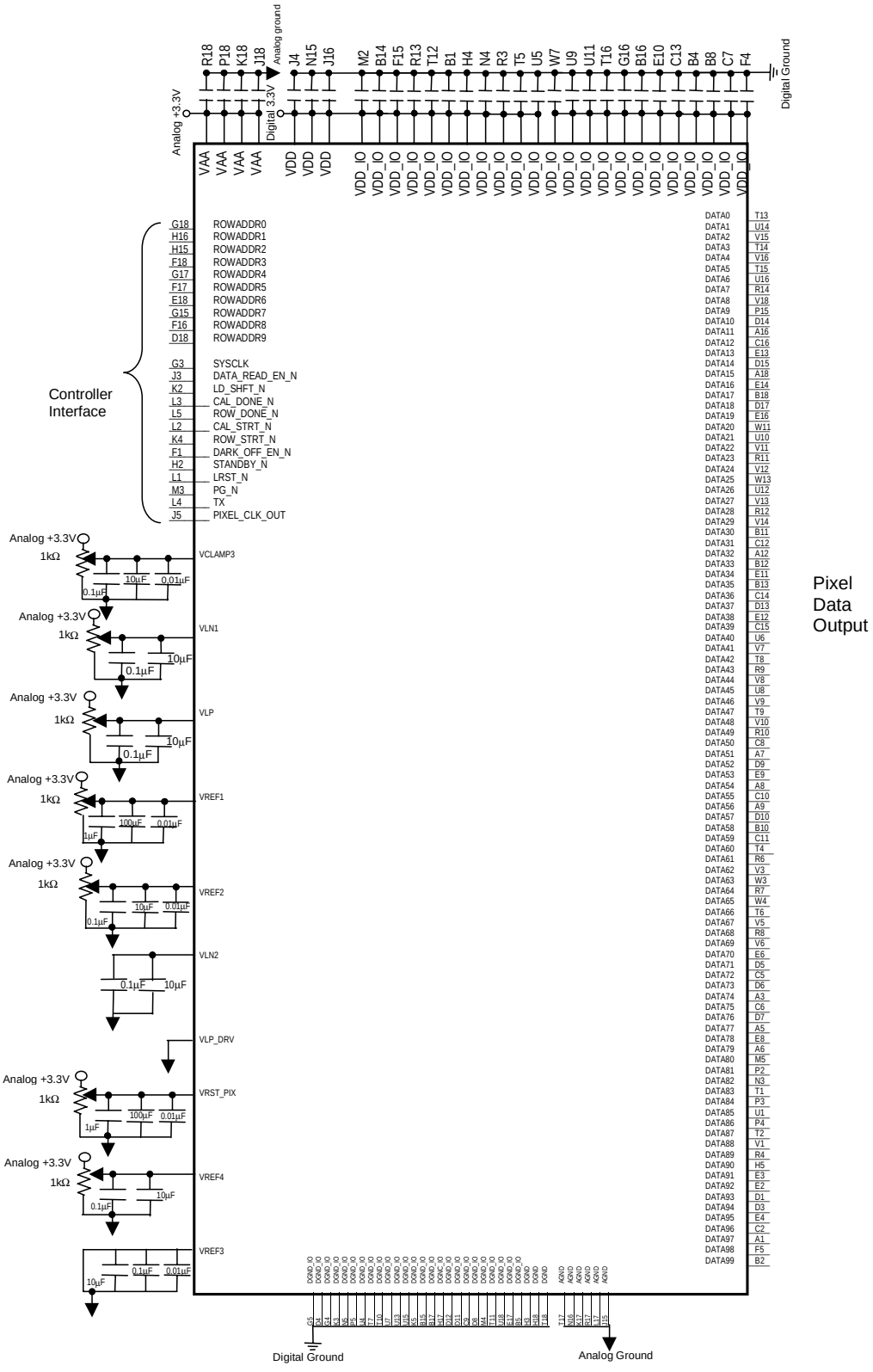
Signal Name	Function	Pin Number(s)
ROW_ADDR4	.....	G17
ROW_ADDR5	.....	F17
ROW_ADDR6	.....	E18
ROW_ADDR7	.....	G15
ROW_ADDR8	.....	F16
ROW_ADDR9	.....	D18
ROW_DONE_N	A two-cycle-wide pulse that indicates that processing of the currently addressed row has been completed.	L5
ROW_STRT_N	Starts ADC conversion of the pixel row (defined by the row address) content. A two-clock cycle-wide active-low pulse.	K4
STANDBY_N	A low input sets the sensor in a low power mode. (Allow 1 microsecond before calibrating, after coming out of this mode). Signal is pulled up on-chip.	H2
SYSCLK	Clock input for entire chip. Maximum design frequency is 70 MHz (50%, ±5%, duty cycle).	G3
VDD_IO	Power supply for digital pad ring.	G16, E10, C13, B4, B8, C7, F4, M2, B14, F15, R13, T12, B1, H4, N4, R3, T5, U5, W7, U9, U11, T16, B16
VLN1	Bias setting for pixel source follower operating current. Impedance: 3kOhm, 10pF. Decoupling capacitors recommended.	L15
VLN2	Bias setting voltage for ADC. Leave open circuit since this current is set on-chip. Impedance: 3kOhm, 10pF.	M18
VLP	Bias setting voltage for the column source follower operating current. Impedance: 3kOhm, 10pF. Decoupling capacitors recommended.	N17
VREF1	ADC reference input voltage that sets the maximum input signal level (defines the level where the FF code occurs) and thus sets the size of the least significant bit (LSB) in the analog to digital conversion process. A smaller VREF1produces a smaller LSB, which means a smaller analog signal level input is required to produce the same digital code out. Likewise, a larger VREF1 produces a larger LSB, which means a larger analog signal level input is required to produce the same digital code out. Thus the reference value can be used like a global gain adjustment. This signal has two pin connections to minimize internal losses during high-speed operation. User voltage source must supply a transient current of 100 mA at a frequency of 500 kHz with a 2% duty cycle. Decoupling capacitors to AGND of ~1µF (ceramic) and 100 µF (electrolytic) placed as close to the package pins as possible are usually sufficient to filter out this required current transient.	K16, M15

2.5 Pin Descriptions (continued)

Signal Name	Function	Pin Number(s)
VREF2	ADC reference used for the calibration operation. User voltage source must supply a transient current of 20 mA at a frequency of 500 kHz with a 2% duty cycle. A ceramic decoupling capacitor to AGND of ~0.1μF is usually sufficient to filter out this required current transient.	P17
VREF3	Dark offset cancellation positive input reference, tied to the pedestal voltage to be added to the signal. Should be connected to AGND.	M16
VCLAMP3	Dark offset cancellation negative input reference. User voltage source must supply a transient current of 40 mA at a frequency of 500 kHz with a 2% duty cycle. A ceramic decoupling capacitor to AGND of ~0.1 μF to 1μF is usually sufficient to filter out this required current transient.	K15
PIXEL_CLK_OUT	Data synchronous output. User may prefer to use this pin as data clock instead of SYSCLK.	J5
DGND_IO	Digital ground for pad ring.	G5, D4, G4, K3, N5, P5, U4, T7, T10, U7, U13, K5, B15, B17, H17, D12, D11, E17, C9, D8, M4, T11, U18, B5, U15
VLP_DRV	Should be connected to AGND.	R16
TX_N	This is an active low pulse that controls transfer of charge from photodietector to memory inside each pixel for entire pixel array.	L4
PG_N	This is an active low pulse that resets the photodetectors and thereby starts new integration cycle.	M3
VRST_PIX	Power supply for pixel array. There is no noticable dc power consumption by this pin (<100 μA). User voltage source must supply a transient current of 10 mA at a frequency of 500 kHz or a few amps, once a frame. Decoupling capacitors to AGND of ~1 μF (ceramic) and 100 μF (electrolytic) are usually sufficient to filter out this required current transient.	L18, P16, J17

Signal Name	Function	Pin Number(s)
VREF4	ADC reference input. User voltage source must supply a transient current of 100 mA at a frequency of 500 kHz with a 2% duty cycle. A ceramic decoupling capacitor to AGND of ~0.1µF is usually sufficient to filter out this required current transient.	L16
—	No connect.	E5,C3,C1, D2, E1, F2, F3, G1, H1, J2, J1, K1, M1, N1, N2, P1,R1, R2, T3, U2, R5, U3, V2, W2, W1, V4, W5, W6, W8, W9, W10,W12, W14, W15,W17, W18, V17, R15, U17, V19, W19, U19, T19, R19, P19, N18, N19, M19, M17, L19, K19, J19, H19, G19, F19, E19, D19, C19, B19, C18, E15, C17, D16, A19, A17, A15, A14, A13, A11, A10, B9, B7, B6, A4, E7, A2, C4, B3, W16, G2

2.6 Board Connections



Notes: 1. It is recommended that 0.01mF and 0.1mF capacitors be placed as physically close as possible to the PB-MV13's package.
2. Alternatively, the analog voltages depicted as being generated from potentiometers could be supplied from DACs.
3. The analog voltages VLN1, VLN2, VLP, and VREF4 are generated on-chip, but user may supply voltages to override the internal biases.

2.7 Electrical Specification

AC Electrical Characteristics (Vsupply = 3.3V ± 0.3V)

Symbol	Characteristic	Condition	Min.	Typ.	Max.	Unit
Tplh	Data output propagation delay for low to high trans.		1	2	3	ns
Tphl	Data output propogation delay for high to low trans.		1	2	3	ns
Tsetup	Setup time for input to CLK	Vin = Vpwr or Vgnd	1	2	3	ns
Thold	Hold time for input to CLK	Vpwr=Min,VOH min		4		ns
PSRR_VDD	Power supply rejection ratio for digital supply	100 mV ripple at 9.7 kHz on supply		TBD		dB
PSRR_VDD_IO	Power supply rejection ratio for digital supply	100 mV ripple at 9.7 kHz on supply		TBD		dB
PSRR_VAA	Power supply rejection ratio for analog supply	100 mV ripple at 9.7 kHz on supply		TBD		dB

DC Electrical Characteristics (Vsupply = 3.3V ± 0.3V)

Symbol	Characteristic	Condition	Min.	Typ.	Max.	Unit
VLP	Bias for Column Buffers		0.5	1.9	2.7	V
VREF1	Reference for ADC		0.2	1.0	1.5	V
VREF2	Reference for ADC Calibration		0.2	0.7	1.5	V
VREF3	Dark offset		0	0	2.5	V
VLN1	Bias for pixel source follower		0.8	1.0	1.2	V
VLN2	Bias for ADC		0.8	Open	1.2	V
VCLAMP3	Dark offset		0	0	3.0	V
VLP_DRV	Row driver control		0	0	2.0	V
VRST_PIX	Pixel Array Power		2.0	2.9	3.0	V
VREF4	Reference for ADC			Open or 0.25		V
VIH	Input High Voltage		2.0		Vpwr+0.3	V
VIL	Input Low Voltage		-0.3		0.8	V
IIN	Input Leakage Current, No Pullup Resistor	Vin = Vpwr or Vgnd	-5		5	µA
VOH	Output High Voltage	Vpwr=Min, IOH=-100µA		Vpwr-0.2		V
VOL	Output Low Voltage	Vpwr=Min, IOL=100µA			0.2	V
Ipwr[1]	Maximum Quiescent Supply Current	66 MHz clock, 5pF load on outputs		165		mA

[1]Ipwr = I (VDD_IO) + I (VDD) + I (VAA)

2.7 Electrical Specification (continued)

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
Vpwr	DC Supply Voltage	-0.5 to 3.6	V
Vin	DC Input Voltage	-0.5 to Vpwr + 0.5	V
Vout	DC Output Voltage	-0.5 to Vpwr + 0.5	V
I	DC Current Drain per Pin (Any I/O)	±50	mA
I	DC Current Drain, Vpwr and Vgnd	±100	mA

Maximum Ratings are those values beyond which damage to the device may occur.
Vpwr = VDD = VAA = VDD_IO (VDD is supply to digital circuit, VAA to analog circuit).
Vgnd = DGND = AGND (DGND is the ground to the digital circuit, AGND to the analog circuit).

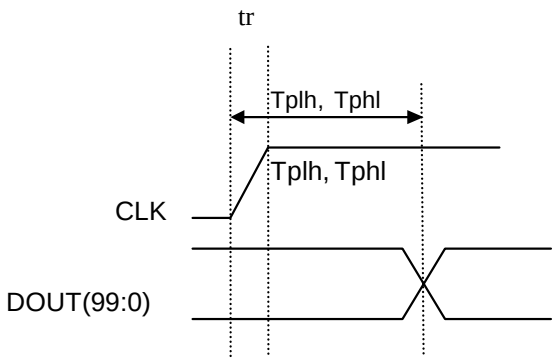
Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
Vpower	DC Supply Voltage	3.00	3.6	V
T_A	Commercial Operating Temperature	-5	60	C
T_J	Junction Temperature	TBD	TBD	C

This device contains circuitry to protect the inputs against damage from high static voltages or electric fields, but the user is advised to take precautions to avoid the application of any voltage higher than the maximum rated.

Power Dissipation (Vpwr = 3.3V; T_A = 25°C @500 fps)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Pavg	Average Power	250	350	500	mW



Clock to Data Propagation Delay

3.0 Optical

3.1 Optical Specification

Image Sensor Characteristics (T_A = 25°C)

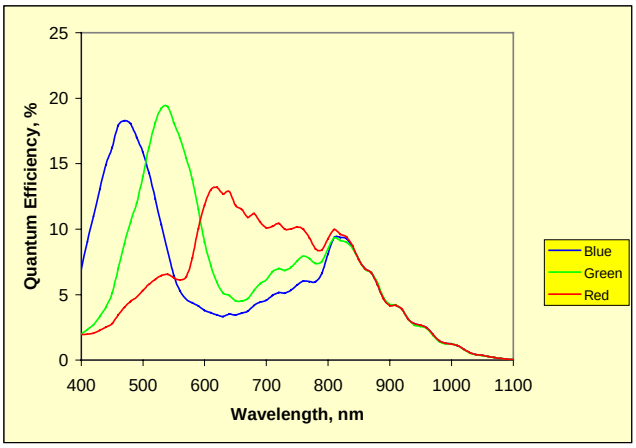
Symbol	Parameter	Typ.	Unit
R_I	Responsivity (ADC VREF=1V)	1000	LSB/lux-sec.
DSNU, HF	Dark signal non-uniformity, high spatial frequency	<0.4	% rms
DSNU, LF	Dark signal non-uniformity, low spatial frequency	<3	% p-p
Vdrk	Output referred dark signal	300	bits/sec
Dyn_I	Internal dynamic range	59	dB
PRNU, HF	Photo response non-uniformity, high spatial frequency	<0.6	% rms
PRNU, LF	Photo response non-uniformity, low spatial frequency	<10	% p-p
Kdrk	Dark current temperature coefficient	100	%/8°C

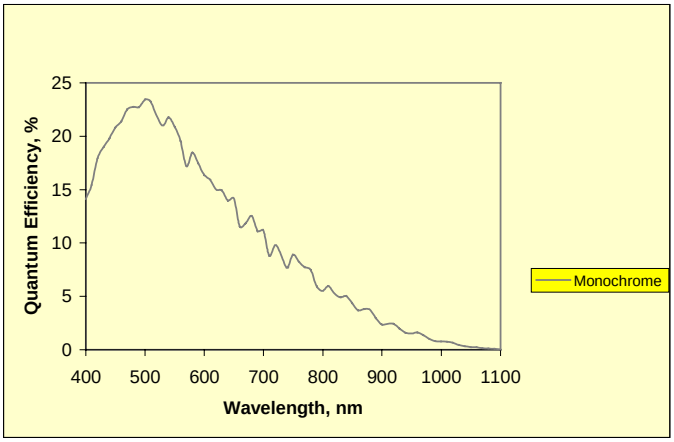
For additional details regarding the defect specifications please contact Photobit.

Pixel Array

Symbol	Parameter	Typ.	Unit
Resolution	Number of pixels in active image	1280 x 1024	pixels
Pixel size	X-Y dimensions	12 x 12	µm
Pixel pitch	Center-to-center pixel spacing	12	µm
Pixel fill factor	Area of drawn active area	40	%

3.2 Quantum Efficiency





Wave-length (nm)	Monochrome Quantum efficiency (%)	Blue Quantum efficiency (%)	Green Quantum efficiency (%)	Red Quantum efficiency (%)
389.9	12.12			
399.9	14.12	6.95	2.00	1.95
409.9	15.46	9.05	2.34	1.98
419.9	17.97	10.99	2.71	2.07
430.0	19.03	13.04	3.35	2.27
440.0	19.82	14.91	4.05	2.51
450.0	20.81	16.23	5.10	2.79
460.0	21.41	17.91	6.99	3.46
469.9	22.50	18.29	8.91	4.05
479.9	22.75	18.06	10.55	4.48
489.9	22.73	17.01	12.01	4.83
499.9	23.44	15.90	14.01	5.31
509.9	23.23	14.28	16.29	5.81
520.0	21.88	12.32	18.14	6.17
530.0	21.01	10.34	19.23	6.45
540.0	21.77	8.32	19.37	6.56
550.0	20.88	6.46	18.12	6.29
560.0	19.55	5.30	16.97	6.12
570.0	17.21	4.65	15.44	6.36
579.9	18.49	4.38	13.81	7.80
589.8	17.49	4.14	11.52	10.05
599.9	16.39	3.80	9.00	11.84
609.9	15.93	3.61	7.23	13.01
619.9	15.01	3.46	5.95	13.19
629.9	14.92	3.34	5.12	12.69
639.9	13.98	3.52	4.95	12.89
649.9	14.16	3.45	4.54	11.83
659.9	11.55	3.59	4.52	11.52
669.9	11.85	3.74	4.69	10.91
679.9	12.51	4.18	5.32	11.18
689.9	11.11	4.42	5.83	10.57
699.9	11.17	4.57	6.15	10.11
709.9	8.80	4.94	6.75	10.22
719.9	9.82	5.16	6.98	10.43
729.9	8.82	5.12	6.87	9.99
739.9	7.67	5.34	7.09	10.02
749.9	8.90	5.74	7.59	10.17
759.8	8.24	6.03	7.95	9.99
769.8	7.74	6.00	7.75	9.32
779.8	7.48	6.00	7.38	8.50
789.8	5.93	6.63	7.54	8.42
799.8	5.50	8.10	8.49	9.25
809.7	5.97	9.36	9.35	9.98
819.7	5.27	9.38	9.13	9.61
829.7	4.92	9.27	9.00	9.41
839.7	5.03	8.64	8.55	8.73
849.7	4.38	7.67	7.67	7.67
859.7	3.69	7.01	6.93	7.01
869.7	3.81	6.69	6.69	6.69
879.7	3.77	5.78	5.91	5.78
889.7	2.96	4.69	4.78	4.69
899.7	2.37	4.22	4.26	4.17
909.7	2.42	4.18	4.22	4.18
919.7	2.44	3.88	3.88	3.88
929.7	1.97	3.14	3.17	3.14
939.7	1.60	2.78	2.68	2.78
949.7	1.52	2.68	2.57	2.67
959.7	1.62	2.47	2.43	2.47
969.7	1.36	1.97	1.90	1.98
979.7	1.03	1.49	1.43	1.49
989.7	0.81	1.30	1.25	1.30
999.7	0.79	1.25	1.25	1.22
1009.7	0.77	1.10	1.11	1.10
1019.7	0.66	0.84	0.80	0.85
1029.7	0.45	0.57	0.54	0.57
1039.6	0.34	0.43	0.41	0.43
1049.6	0.25	0.37	0.35	0.37
1059.6	0.23	0.28	0.28	0.28
1069.6	0.16	0.20	0.19	0.20
1079.6	0.13	0.13	0.12	0.13
1089.6	0.08	0.08	0.08	0.09
1099.6	0.05	0.06	0.06	0.07

3.3 Lens Selection

Much of the specific information in this section is explained in detail in the Technology section on the Photobit website. The following information applies specifically to the Photobit PB-MV13 megapixel image sensor.

Format

The diagonal of the image sensor array, 19.67 mm, fits most closely, but not exactly, within the optical format corresponding to the 1-inch specification. Some 1-inch optical format lenses have been shown to work well with this sensor.

Mounting

Several lens mounting standards exist that specify the threading of the lens' barrel as well as the distance the back flange of the lens should be from the image sensor for the lens to properly form an image. Typical lens mounting standards for the PB-MV13 are:

Mount Name	Mounting Threads	Back-Flange-to-Image-Sensor
C	1 - 32	17.526 mm
CS	1 - 32	12.5 mm

Field of View and Focal Length

The field of view of an imaging system will depend on both the focal length of the imaging lens and the width of the image sensor. As most of the image information humans pay attention to generally falls within a 45-degree horizontal field of view, many camera systems attempt to imitate this field of view. However, in some cases a telephoto system (with a narrow field of view, say less than 20 degrees), or a wide angle system (with a wide field of view, say more than 60 degrees) may be desired. The approximate field of view that an imaging system can achieve is shown in the following equation:

$$\theta \approx 2\tan^{-1}\left(\frac{w}{2f}\right)$$

where θ is the field of view, $\tan^{-1}$ is the trigonometric function arc-tangent, w is the width of the image sensor, and f is the focal length of the imaging lens. For example, the imaging system's diagonal field of view can be determined by using the diagonal of the image sensor (19.67 mm) for w and a particular lens' focal length for f. Alternatively, the imaging system's horizontal field of view can be determined by using the horizontal of the image sensor (15.36 mm) for w and a particular lens' focal length for f. A lens with an approximately 50 mm focal length will provide a n 18-degree horizontal field of view with a PB-MV13 (keep in mind that the above equation is a simplified approximation).

F-Number

The f-number, or f/#, of an imaging lens is the ratio of the lens' focal length to its open aperture diameter. Every doubling in f-number reduces the light to the sensor by a factor of four. For example, a lens set at f/1.4 lets in four times more light than that same lens when it is set at f/2.8. Low f-number lenses capture a lot of light for delivery to the image sensor, but also require careful focus. Higher f-number lenses capture less light for delivery to the image sensor, and do not require as much effort to bring the imaging system to focus. Low f-number lenses generally cost more than high f-number lenses of similar overall performance. Typical f-numbers for various imaging systems are:

F-#	Imaging application
1.4	Low-light level imaging, manual focus systems
2.0	Typical for PC and other small form cameras
2.8	Common in digital still cameras
4.0+	Often used in machine vision applications

Typical f-numbers will range from 1.8 to 2.8. For example, most S-mount lenses come with a fixed f-number of f/2.0.

3.3 Lens Selection (continued)

MTF

Modulation Transfer Function (MTF) is a technical term that quantifies how well a particular system propagates information. For cameras, the "system" is the lens and the sensor, and the "information" is the picture they are capturing. MTF ranges from zero (no information gets through) to 100 (all information gets through), and is always specified in terms of information density. In most imaging systems, the MTF is limited by the performance of the imaging lens. A lens must be able to transfer enough information to the image sensor to be able to resolve details in the image that are as small as the pixels in the image sensor. The pixels are set on a 12-micron pitch (the center of one pixel is 12 microns from the center of its neighboring pixel). Thus, a lens used should be able to resolve image features as small as 12 microns. Typically, a lens' MTF is plotted as a function of the number of line pairs per millimeter the lens is attempting to resolve (more line pairs per millimeter mean higher information densities). For an electronic imaging system, one line pair will correspond to two image sensor pixels (each pixel can resolve one line). This is equated as:

$$LP/mm = \frac{1}{2z}$$

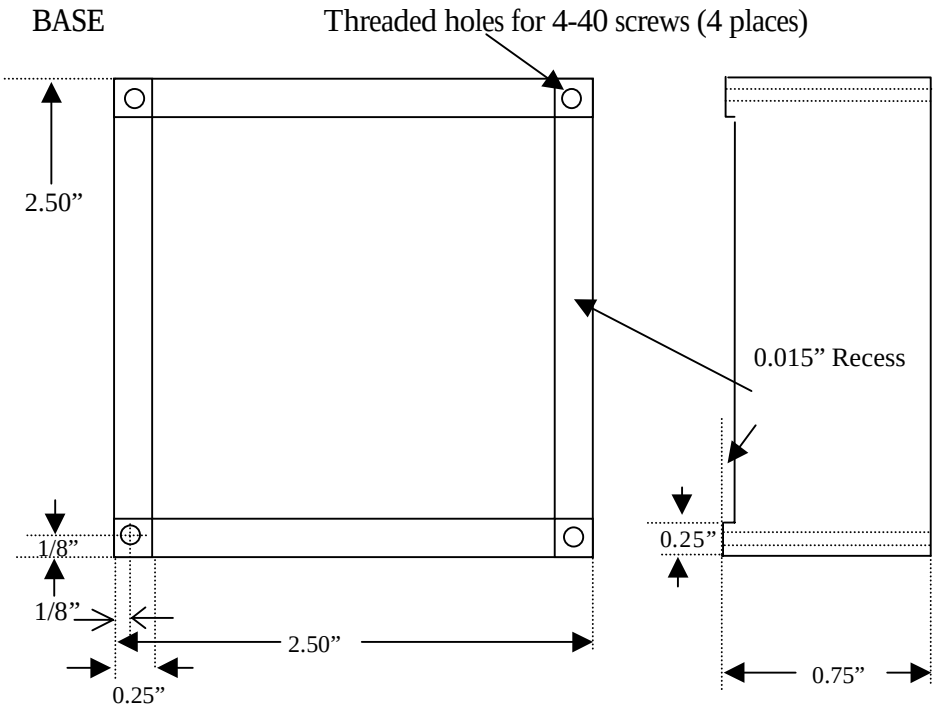
where LP/mm means line pairs per millimeter and z is the image sensor's pixel pitch, in millimeters. For the PB-MV13, z = 0.012 mm, such that the PB-MV13 has 42 LP/mm. Thus, a lens should provide an acceptable level of MTF all the way out to 42 LP/mm. For most lenses, the MTF will be highst in the center of the images they form, and gradually drop off toward the edges of the images they form. As well, MTFs at low values of LP/mm will generally be larger than MTFs at high values of LP/mm. One of the many trade-offs that must be decided by the end user is how high the MTF needs to be for a particular imaging situation. Generally, near an image sensor's LP/mm good MTFs are higher than 40, moderate MTFs are from 20 to 40, and poor MTFs are less than 20.

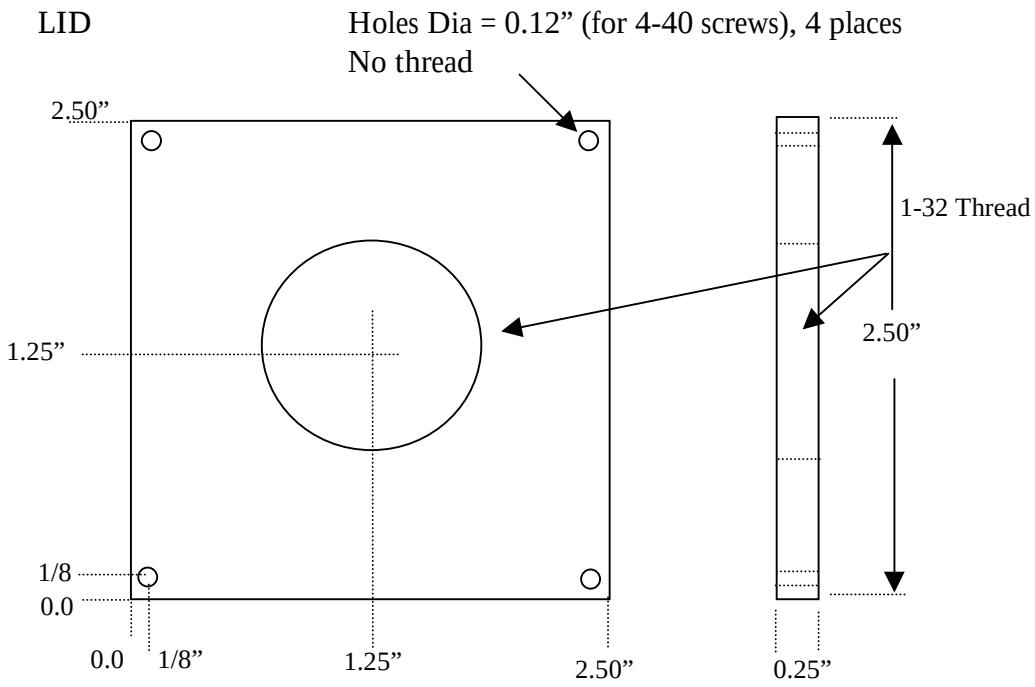
Infrared Cut-Off Filters

In most visible imaging situations it is necessary to include a filter in the imaging path that blocks infrared (IR) light from reaching the image sensor. This filter is called an IR cut-off filter. Various forms of IR cut-off filters are available, some absorptive (like Hoya's CM500 or Schott's BG18) and some reflective (i.e., dielectric stacks). Infrared light poses a problem to visible imaging because its presence blurs and decreases the MTF in the images formed by a lens. Since human vision only extends across a narrow range of the electromagnetic spectrum, camera systems hoping to capture images that look like the images our eyes capture must not capture light outside of our vision range. Silicon-based light detectors (like the ones in the PB-MV13's pixels) detect light from the very deep blue to the near infrared. Thus, a filter must exist in the light's path that keeps the infrared from reaching the image sensor's pixels. In most cases, it is important that such a filter begin blocking light around 650 nm (in the deep red) and continue blocking it until at least 1100 nm (in the near IR). In most camera systems, the IR cut-off filter is included in the imaging lens. However, this point must be verified by a lens vendor when a particular lens is chosen for use with an image sensor.

C-Mount Lens Shroud for PB-MV13 and Socket

Note: This shroud is designed to accommodate the PB-MV13 when it is inserted into a PGA socket. These dimensions are based on the MILL MAX #510-93-281-19-081003 socket (www.mill-max.com).

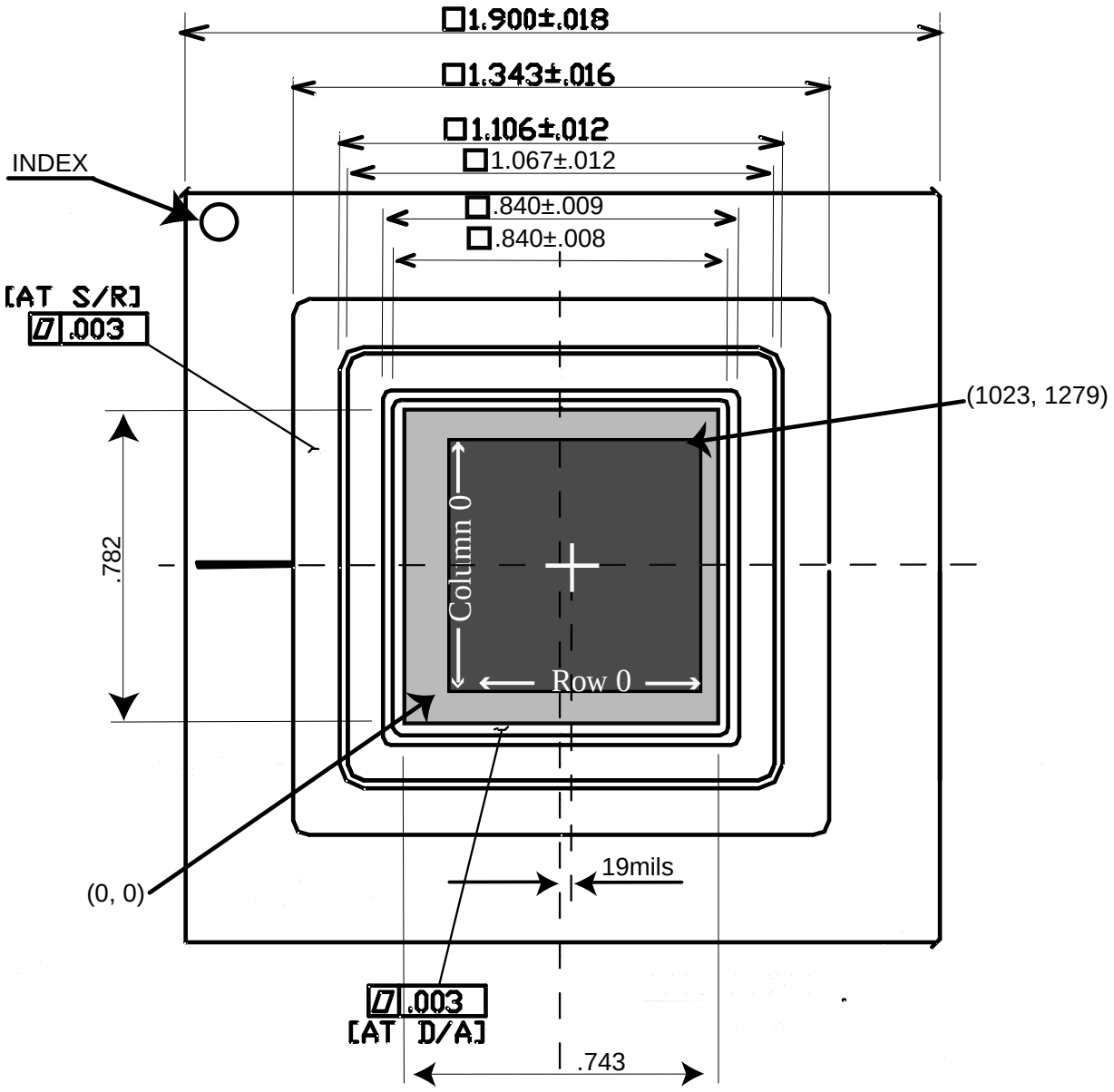




4.0 Mechanical

4.1 Package (280-Pin Ceramic PGA)

Top View

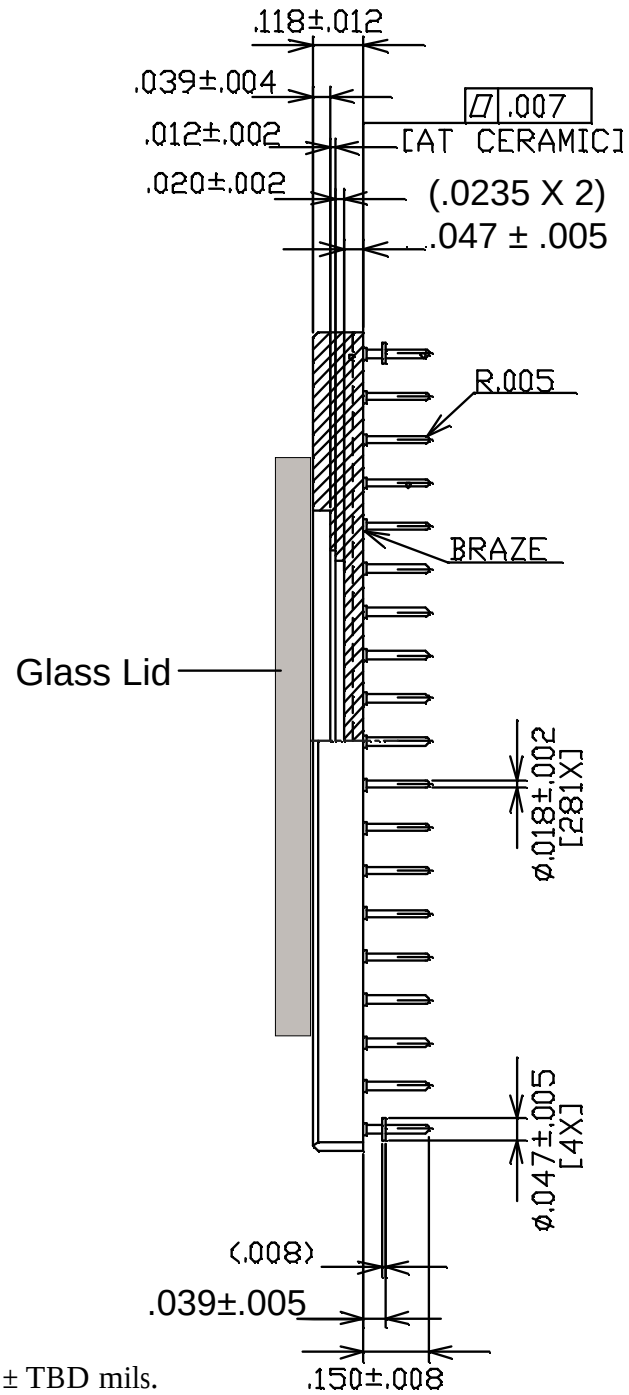


UNITS: INCHES EXCEPT WHERE NOTED

Notes:

1. Gold Plate 60m inches minimum over 50~350m inches nickel.
2. Sensor is centered on package, pixel array is off-center.

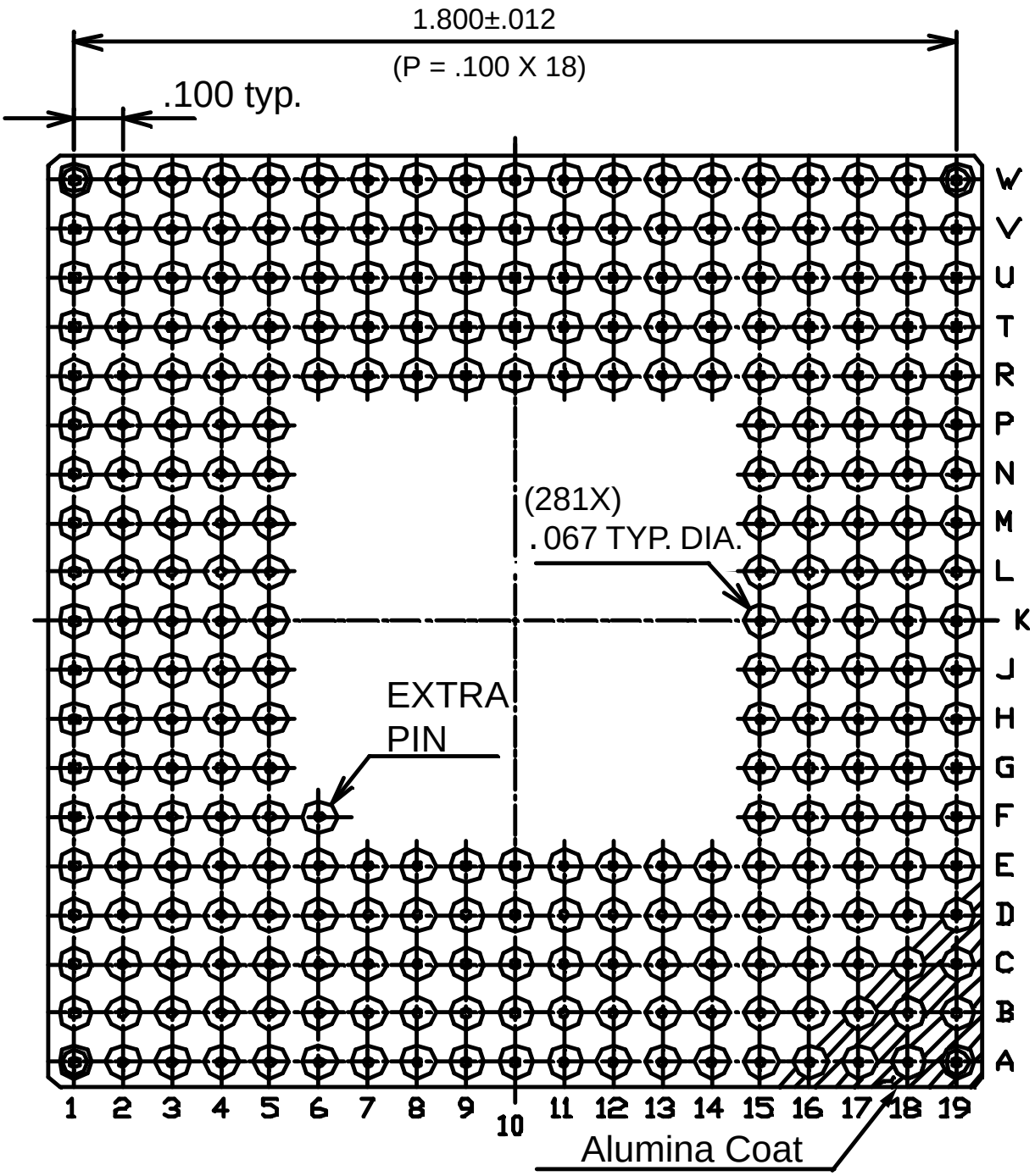
Side View



Notes:
1. Die thickness TBD mils ± TBD mils.
2. D-253 glass lid thickness 31±2 mils.
3. Glass lid epoxy thickness TBD mils ± TBD mils.

4.1 Package (280-Pin Ceramic PGA) (continued)

Bottom View



UNITS: INCHES

TBD

5.0 Environmental

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
Tstorage	Storage Temperature Range	-40 to 125	C
Tlead	Lead Temperature (10 second soldering)	235 max.	C